

PTO-1449	Application No. 09/870,460	Applicant(s): MICHAEL I. CATHERWOOD	
Information Disclosure Citation in an Application	Docket Number 068354.1468	Group Art Unit 2131	Filing Date June 1, 2001

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
A	5701493	12/23/91	Jaggard	395	734	8/3/95
B	5386363	1/31/95	Thomas, deceased	395	650	10/13/92
C	6694398	2/17/04	Zhao et al.	710	260	4/30/01
D	5623646	4/22/97	Clarke	395	360	9/12/95
E	4709324	11/24/87	Kloker	364	200	11/27/85
F	5561384	10/1/96	Reents et al.	327	108	11/8/95
G	5450027	9/12/95	Gabara	326	98	4/8/94
H	4945507	7/31/90	Ishida et al.	708	330	6/12/89
I	3930253	12/30/75	Matda	340	347	1/24/74
J	6728856	4/27/04	Grosbach et al.	711	202	6/1/01
K	6282637	8/28/01	Chan et al.	712	223	12/2/98
L	6055619	4/25/00	North et al.	713	36	2/7/97
M	5974549	10/26/99	Golan	713	200	3/27/97

FOREIGN PATENT DOCUMENTS

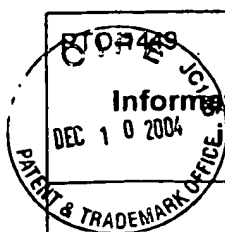
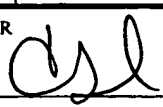
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
un	N 01037124 A	2/1989	JP (w/abstract)	H03M	001/82		X
un	O 0 554 917 A2	8/11/93	EP	G06F	9/26	X	
	P 96/11443	4/18/96	WO	G06F	15/78	X	
un	Q 0 855 643 A1	07/29/98	EP	G06F	9/30	X	
un	R 0 992 888	12/04/00	EP	G06F	9/32	X	
un	S 0 992 889	12/14/00	EP	G06F	9/32	X	

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un	T	Moon B I et al.: "A 32-bit RISC Microprocessor with DSP Functionality: Rapid Prototyping" IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Institute of Electronics Information and Comm. Eng. Tokyo, JP, vol. E84-A no. 5, pages 1339-1347, XP001060025 ISSN: 0916-8508		May 2001
un	U	Turley J: "Balancing Conflicting Requirements When Mixing RISC, DSPs" Computer Design, Pennwell Publ. Littleton, Massachusetts, US, vol. 37, no. 10, pages 46, 48, 50-53, XP000860706 ISSN:0010-4566		October 1998
un	V	Levy M: "Microprocessor and DSP Technologies Unite for Embedded Applications" EDN Electrical Design News, Cahners Publishing Co., Newtown Massachusetts, US, no. Europe, pages 73-74, 76, 78-80, XP000779113 ISSN: 0012-7515		2 March 1998
un	W	Intel, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, Pages 3-1, 3-2, 3-15, 14-1 to 14-30, 18-7, and 25-289 to 25-292		1995



W	X	Intel, Embedded Intel486 Processor Family Developer's Manual, pgs. 2-2, 3-17, 3-37, 4-5, 4-6, 10-1 to 10-12, 12-1 to 12-10	10/1997
W	Y	Moore, M "Z80 Family Interrupt Structure". Barleywood (online), retrieved from the internet <URL: http://www.gaby.de/z80/1653.htm >	1997
W	Z	PCT Search Report based on PCT/US02/16706, 6 pages	Mailed 9/27/02
	AA	PCT Search Report based on PCT/US02/16705, 7 pages	Mailed 9/9/02
W	BB	PCT Search Report based on PCT/US02/16921, 4 pages	Mailed 10/18/02
	CC	SPARC, International, Inc., "The SPARC Architecture Manual", Version 8, pp 1-303	1992
W	DD	Weaver, et al., SPARC International, Inc. "The SPARC Architecture Manual", Version 9, pp. xiv, 137, 146-147, 200-204, 221-222, 234-236, 299	1994-2000
W	EE	Free On-Line Dictionary of Computing (FOLDOC). http://wombat.doc.ic.ac.uk/foldoc/ Search term: program counter	1995
EXAMINER		DATE CONSIDERED	
CSL		5/21/05	
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.			

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		09/870,460		Catherwood			
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		068354.1468		2131		June 1, 2001	
U.S. PATENT DOCUMENTS							
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
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<input type="checkbox"/>	B.						
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FOREIGN PATENT DOCUMENTS							
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EXAMINER					DATE CONSIDERED		
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